REMARKS

Claims 1-25 are presented for further examination. Claims 1, 3, 4, 15, 17, and 24 have been amended. Claim 25 is new.

In the Office Action mailed February 14, 2006, the Examiner rejected claims 1-4, 15-17, and 24 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,831,566 ("Ginetti"). Claims 18 and 19 were rejected under 35 U.S.C. § 103(a) as obvious over Ginetti in view of applicant's admitted prior art. Claims 20-23 were rejected as obvious over Ginetti in view of U.S. Patent No. 5,844,515 ("Park"). Claims 5-14 were found to be allowable.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

Response to Rejections Over the Art

In remarks accompanying the rejection, the Examiner maintained that Ginetti disclosed a selection and deselection circuit in the plurality of transistors 130 coupled to the outputs of the decoder 120. The Examiner referenced column 4, lines 33-41 of Ginetti and Figure 2 in support of the position that the claimed "selected output is used to deactivate the plurality of outputs that are not selected" is met in the plurality of transistors 130 in Ginetti. To more clearly define the invention, claim 1 has been amended to indicate that the selection means activates a single selected output from a plurality of outputs corresponding to an input binary value, and that the deselecting means utilizes the single selected output to deactivate nonselected outputs when the single selected output is activated by forcing the nonselected output to a reference potential. This clearly is not taught or suggested in Ginetti.

More particularly, Ginetti clearly teaches at column 4, lines 33-38, that the output of the decoder is used "to control the opening and closing of the transistor switches 130" [emphasis added]. Thus, the output lines of the decoder do not control the other output lines of the decoder. Rather, they are used to control the NMOS transistor switches. "The decoder 120

has output lines 122 through 125 that control the NMOS transistor switches MN3 through MN0. Output lines 126 through 129 control the operation of the PMOS transistors MP3 through MP0."

Nowhere does Ginetti teach or suggest using a selected output to turn off nonselected outputs. Rather, as set forth at column 4, lines 51-53, "the decoder is used to turn on exactly one of the NMOS switches and exactly one of the PMOS switches."

Even if one were to dispense with one set of the transistor switches, Ginetti teaches turning on only one set of switches and does not teach or suggest turning off nonselected switches. As set forth at column 4, lines 60-66, "it is also contemplated that one may dispense with one set of the transistor switches. For example, if R2 were connected directly to V_{SS} instead of through switch MN1, then the NMOS switches may be dispensed with. The decoder would then only switch in V_{DD} through the PMOS transistors to the resister string in order to vary the voltage at V_{OUT}."

Ginetti further teaches having more than one output active at a time and even where one output only is active, Ginetti does not teach or suggest using that one active output to deactivate nonselected outputs by forcing the nonselected output to a reference potential.

For the foregoing reasons, applicant respectfully submits that claim 1 is allowable.

Dependent claims 2 and 3 are allowable for the features recited therein as well as for the reasons why claim 1 is allowable. Claim 3, in particular, recites inactivating the nonselected outputs by coupling the nonselected outputs to the reference potential. Nowhere does Ginetti teach or suggest such a deactivation of its outputs.

Independent claim 4 is directed to a method for providing an improved binary decoder that comprises providing selection means for activating from a plurality of outputs a single selected output corresponding to an input binary value and providing a deselecting means coupled to the plurality of outputs that utilizes the single selected output to deactivate the nonselected outputs of the selection means when the single selected output is activated.

As applicant has previously argued, Ginetti teaches a decoder 120 without providing any details as to the internal circuitry of the decoder. Nowhere does Ginetti teach or suggest a decoder having both a selection and a deselection circuit as set forth in claim 4 or any method for providing the same. Applicant respectfully submits that claim 4 is allowable for these reasons as well as for the reasons why claim 1 is allowable.

Independent claim 15 is directed to a binary decoder having both a selection circuit and a deselection circuit that, *inter alia*, selects a single output and uses the single selected output to deactivate nonselected outputs by forcing the nonselected outputs to a reference voltage. Applicant respectfully submits that claim 15 is allowable for the reasons why claim 1 is allowable.

Dependent claims 16-24 all depend from claim 15 and are allowable for the features recited therein as well as for the reasons why claim 15 is allowable. More particularly, claim 24 has been amended to recite the third and fourth transistors having control terminals coupled to the second and first outputs, respectively. Nowhere does Ginetti teach or suggest such a transistor configuration.

Claim 25, which depends from claim 24, recites two additional transistors of the selection circuit. Thus, claim 25 is comparable to allowable claim 5. Applicant respectfully submits that claim 25 is allowable for the reasons why claim 5 is allowed.

In view of the foregoing, applicant submits that all of the claims in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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